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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,832	10/29/2003	Jaemin Lim	Q76050	9459

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,832	LIM ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments to Claims 3, 5, 8, 12, and 13 have been acknowledged. The 35 U.S.C. 112, second paragraph rejections have been overcome and are therefore withdrawn.

2. The amendments to Claims 6 and 9-11 have been acknowledged.

3. Claim 7 has been canceled by the Applicant.

4. Claims 1-6 and 8-13 stand rejected.

Claim Rejections - 35 USC § 102

5. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 1-4, 6 and 8-13 are rejected under U.S.C. 102(e) as being anticipated by Tang et al. (US PGPUB: 2003/0206442 A1)

Claim 1. An apparatus *(Abstract, line 1 – Declares a flash memory bridging device (a.k.a. apparatus)* for controlling execute-in-place (XIP) in a serial flash,

comprising: *(Section 0009, lines 7-10 – State that the NAND Flash Memory (a.k.a. Serial Flash) is supported by XIP)*

- a cache module for accessing a designated memory address of the serial flash *(Abstract, lines 4-6 – State that "a cache control logic" (a.k.a. cache module) "is used to determine if the requested data is a cache hit")*
- in response to a command received from a main control unit *(Section 0008, lines 23-29 – State that the "main control unit" controls the writing of data "into the NAND flash memory")*
- through a system interface unit, *(Section 0023, lines 11-14 – Declare a "control logic unit" (a.k.a. system interface unit))*
- and reading or writing data required by the main control unit in a read or write operation; *(Section 0008, lines 23-28 – State that the main control unit reads and writes data)*
- a serial flash controller *(Section 0008, line 19 – Declares that there is a NAND flash memory control unit (a.k.a. serial flash controller))*
- with a boot loader for allowing system booting to be performed by reading boot codes written on the serial flash, *(Section 0025, lines 6 – State that "the control logic unit (a.k.a. boot loader) will download boot codes from the NAND flash memory to the buffer region")*
- storing the boot codes in a buffer *(Section 0009, lines 8-9 – State that the "boot code is first transferred into the buffer region")*
- and immediately transmitting the boot codes to the main control unit when the main control unit requires the boot codes; *(Section 0026, lines 1- 5 – State that the memory is directed into the main control unit when it is requested)*
- and a flash interface unit for handling transmission and reception of data among the cache module, the serial flash controller and the serial flash. *(Section 0024 – Thoroughly describes the "control logic unit" (a.k.a. flash interface unit))*

Claim 2. The apparatus as claimed in claim 1, wherein the cache module comprises:

- a cache controller that if the read operation is required by the main control unit, accesses the serial flash, *(Section 0011, lines 10-14 – State that the flash memory bridging device accesses the serial flash if required during a read operation)*
- reads a page to which the designated memory address belongs, and transmits data in the read page corresponding to the designated memory address to the main control unit; *(Section 0026, lines 1-10 – Explain the process of reading and transmitting data to the correct memory address)*
- a tag-storing unit on which storage information on the read page is written in response to an operation control of the cache controller;

(Section 0028, lines 20-22 – State that the flash memory bridging device stores the data in response to a write command)
- and a data-storing unit on which the read page is written. *(Section 0027, line 4 – States that the data (read page) is written onto the NAND flash memory, which acts as a data storing unit)*

Claim 3. (AMENDED) The apparatus as claimed in claim 2,
- wherein the cache controller further includes a function of extracting relevant data from the data-storing unit *(Section 0028, lines 27-31 – Describe how data is extracted from the NAND flash memory)*
- and transmitting the extracted data to the main control unit if the page including the designated memory address is written on the tag-storing unit, *(Section 0026, lines 1-5 – State that the data is retrieved by the main control logic unit if the data is in the buffer region)*
- by referring to the tag-storing unit and the data-storing unit upon performing the read operation. *(Section 0028, lines 16-18)*

Claim 4. The apparatus as claimed in claim 1, wherein the serial flash controller further comprises a prefetch for reading beforehand data expected to be required by the main control unit from the serial flash, storing the data in the buffer and immediately providing the data to the main control unit when the main control unit requires the data. *(Section 0026, lines 9-14 – State that the NAND flash memory control unit uses an error correction code unit to pre-read data that is to be written into the buffer region (which will ultimately move into the main control unit)*

Claim 6. (AMENDED) A flash memory chip having an apparatus for controlling execute-in-place (XIP) in a serial flash, the apparatus comprising: *(Section 0010, lines 1-5 –State that the memory control chip (a.k.a. flash memory chip) has the flash memory bridging device for controlling XIP in a NAND flash)*
- a serial-cell type serial flash; *(Section 0010, lines 3-4 – State that there exists a NAND flash memory)*
- and a controller for accessing the serial flash, *(Section 0010, line 4 – Declares that there exists a flash memory bridging device)*
- and directly providing boot codes for system booting which are stored beforehand in a buffer, *(Section 0026, lines 9-14 – State that the NAND flash memory control unit uses an error correction code unit to pre-read data (boot codes) that is to be written into the buffer region (which will ultimately move into the main control unit)*
- or reading or writing relevant data by accessing a designated memory address, in response to an operation required by a main control unit of a system, *(Section 0026, lines 1- 5 – State that the memory is directed into the main control unit when it is requested)*

- wherein the controller comprises:
- a cache module for accessing a designated memory address of the serial flash *(Abstract, lines 4-6 – State that "a cache control logic" (a.k.a. cache module) "is used to determine if the requested data is a cache hit")*
- in response to a command received from a main control unit *(Section 0008, lines 23-29 – State that the "main control unit" controls the writing of data "into the NAND flash memory")*
- through a system interface unit, *(Section 0023, lines 11-14 – Declare a "control logic unit" (a.k.a. system interface unit))*
- and reading or writing data required by the main control unit; *(Section 0008, lines 23-28 – State that the main control unit reads and writes data)*
- a serial flash controller *(Section 0008, line 19 – Declares that there is a NAND flash memory control unit (a.k.a. serial flash controller))*
- with a boot loader for allowing system booting to be performed by reading boot codes written on the serial flash, *(Section 0025, lines 6 – State that "the control logic unit (a.k.a. boot loader) will download boot codes from the NAND flash memory to the buffer region")*
- storing the boot codes in a buffer *(Section 0009, lines 8-9 – State that the "boot code is first transferred into the buffer region")*
- and immediately transmitting the boot codes to the main control unit when the main control unit requires the boot codes; *(Section 0026, lines 1- 5 – State that the memory is directed into the main control unit when it is requested)*
- and a flash interface unit for handling transmission and reception of data among the cache module, the serial flash controller and the serial flash. *(Section 0024 – Thoroughly describes the "control logic unit" (a.k.a. flash interface unit))*

Claim 8. (AMENDED) A method for controlling execute-in-place (XIP) in a serial flash, comprising:

- accessing the serial flash,
- reading boot codes for initial booting, *(Section 0025, lines 6 – State that "the control logic unit (a.k.a. boot loader) will download boot codes from the NAND flash memory to the buffer region")*
- and storing the boot codes in a buffer, when power is supplied to a system; *(Section 0009, lines 8-9 – State that the "boot code is first transferred into the buffer region")*
- if the boot codes are completely stored and the boot codes are required by a main control unit of the system, reading the boot codes from the buffer, *(Section 0023, lines 5-8 – State that "the buffer region may have a plurality of buffering devices such as FIFO or RAM for holding a portion of the address data of the NAND flash memory")*

- transmitting them to the main control unit and processing an operation required by the main control unit; *(Section 0026, lines 1- 5 – State that the memory is directed into the main control unit when it is requested)*
- receiving a data read command *(Section 0008, lines 23-25 – State "The main control unit controls the reading from the NAND flash memory data")*
- together with a memory address for data transmitted in response to a predetermined data read request of the main control unit; *(Section 0024, lines 23-24 – State that the block address translation table is for reading, so inherently there must be a memory address requested)*
- searching the memory address from a tag-storing unit of the controller in response to the received read command; *(Section 0028, lines 11-20 – Demonstrate how the data is searched for by the flash memory bridging device. The data will inevitably have a memory address)*
- if the memory address is found, extracting relevant data from a data-storing unit of the controller and transmitting the data to the main control unit; *(Section 0028, lines 14-16 – State "If the requested data is in the flash memory bridging device, step S450 is executed to respond to the memory read instruction.)*

Claim 9. (AMENDED) The method as claimed in claim 8, wherein the step of reading the boot codes and transmitting them comprises:

- receiving a boot code read command from the main control unit; *(Section 0008, lines 23-25 – State "The main control unit controls the reading from the NAND flash memory data")*
- reading the boot codes stored in the buffer in response to the received boot code read command; *(Section 0008, lines 26-27 – State that the main control unit determines whether the data is already stored in the buffer region)*
- and transmitting the read boot codes to the main control unit. *(Section 0026, lines 1- 5 – State that the memory is directed into the main control unit when it is requested)*

Claim 10. (AMENDED) The method as claimed in claim 8, further comprising:

- receiving a serial flash ID read command transmitted in response to a serial flash ID read request of the main control unit; *(Section 0026, lines 1-3 – State that the main control unit requests and receives a memory read instruction)*
- accessing the serial flash through the cache module of the controller in response to the received serial flash ID read command; *(Section 0026, lines 9-10 – State that "data is read from then NAND flash memory through the NAND flash memory control unit")*
- and reading an entire page to which the serial flash ID required by the main control unit belongs from the serial flash, storing it in the buffer,

and sequentially transmitting required data. *(Section 0026, lines 9-15 – State that the data is read, stored in the buffer, and transferred)*

Claim 11. (AMENDED) The method as claimed in claim 8, further comprising:
- receiving a data write command *(Section 0027, line 1 – States that a memory write instruction is received from the main control unit)*
- together with a memory address for data transmitted in response to a predetermined data write request of the main control unit; *(Section 0024, lines 23-24 – State that the block address translation table is for writing, so inherently there must be a memory address requested)*
- storing the data transmitted from the main control unit in the buffer in response to the received data write command; *(Section 0027, lines 1-2 – State that the write-in data is transferred to the buffer region)*
- and writing the data stored in the buffer on a memory address assigned by a means for mapping the serial flash. *(Section 0024, lines 23-24 – State that the block address translation table is for writing, so inherently there must be a memory address to which the serial flash is mapped))*

Claim 12. (AMENDED) The method as claimed in claim 8, further comprising:
- if the memory address is not found, accessing the serial flash, reading a page to which the memory address belongs, storing the page in the buffer, extracting data at the memory address, and transmitting the data at the memory address to the main control unit. *(Section 0028, lines 16-20 – State "if the requested data is not in the flash memory bridging device, Step S440 is executed to read the data from the NAND flash memory before executing step S450 to respond to the memory read instruction")*

Claim 13. (AMENDED) The method as claimed in claim 12, wherein the step of accessing the serial flash, reading the page to which the memory address belongs, storing the page in the buffer, extracting the data at the memory address, and transmitting the data at the memory address to the main control unit further comprises writing storage information on the read page on the tag-storing unit and writing the read page on the data-storing unit. *(Section 0028, lines 9-24 – State that the storage information on resides on the flash memory bridging device and writes the storage information in response to the memory read instruction to the NAND flash memory. Section 0026, lines 1-10 – Explain the process of reading and transmitting data to the correct memory address. Section 0027, line 4 – States that the data (read page) is written onto the NAND flash memory, which acts as a data storing unit)*

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C.103(a) as being unpatentable over Tang et al. as applied to claim 2 above, further in view of M-Systems' article in Home Toys E-Magazine, entitled "One Chip Does it All" (hereafter referred to as M-Systems)

Tang teaches the limitations of claim 2 for the reasons above.

Tang's invention differs from the claimed invention in that there is no specific reference to "SRAM".

Tang fails to teach (AMENDED) claim5, which states "The apparatus as claimed in claim 2, wherein the data-storing unit and the tag-storing unit are SRAM." However, M-Systems discloses "SRAM" (page 4, line 4).

It would have been obvious to one of ordinary skill in the art, having the teachings of Tang and M-Systems et al. before him at the time the invention was made, to make use of SRAM as taught by the execute-in-place apparatus of M-Systems, in Tang's execute-in-place apparatus because cache memory is made up of RAM, which includes both DRAM and SRAM (which is faster and more reliable than DRAM), as taught by M-Systems.

Response to Arguments

9. With regards to Claim 1, the Applicant alleges "Tang fails to disclose or suggest the claimed system interface unit and the claimed flash interface unit". However, Tang discloses "The main control logic unit is coupled to the first buffer access unit, the second buffer access

unit and the block address translating table unit" (Section 0008, lines 21-23). Tang further states "The control logic unit 320 is coupled to the buffer region 310 for receiving memory instructions, determining the content of the instruction, executing the instruction and responding to the request demanded by the instruction" (Column 0023, lines 11-14). The Applicant discloses in the Specification that the "controller 500 mainly comprises a system interface unit 510 for transmitting and receiving signals to/from the main control unit 300" (Paragraph 41, lines 1-3). Therefore, the "system interface unit" is taught by Tang.

Tang also teaches that "FIG. 3 is a block diagram showing various components inside a flash memory bridging device according to one preferred embodiment of this invention. As shown in FIG. 3, a flash memory bridging device 300 includes a buffer region 310 and a control logic unit 320. The buffer region 310 may have a single or a plurality of buffering devices such as FIFO or RAM for holding a portion of the address data of the NAND flash memory 230. If the buffer region includes several buffering devices, an interleave access mode may be employed to boost system performance. The control logic unit 320 is coupled to the buffer region 310 for receiving memory instructions, determining the content of the instruction, executing the instruction and responding to the request demanded by the instruction" (Section 0023, lines 1-14). Therefore, since the control logic unit is part of a flash memory scheme, the fact that it is a "flash interface unit" holds true.

As per the evidence above, Tang does in fact disclose the two separate claim elements in Claim 1. Therefore, the Applicant's arguments are moot in view of the prior art.

10. With regards to Claim 1, the Applicant further alleges that the "NAND flash memory control unit 350, however, is part of the control logic unit 8", and does not correspond to the

claimed serial flash controller. Tang discloses however that "On starting the system, the control logic unit 320 will download boot codes from the NAND flash memory 230 to the buffer region 310 so that an execution in place (XIP) function is provided" (Section 0025, lines 4-7). Those (by definition in the Applicant's Specification) are the functions of the serial flash controller. Therefore, the Applicant's arguments are moot in view of the prior art.

11. With regards to Claim 2, the Applicant alleges that "Tang fails to disclose or suggest a cache module comprising a tag-storing unit. Although the Examiner states that the flash memory bridging device stores the data in response to a write command in Tang, there is nothing in Tang which discloses or suggests that storage information on the read page is written on the flash memory bridging device". Tang discloses "The bridging method of claim 15, wherein any error in the data read from the NAND flash memory is corrected before sending to the flash memory bridging device" (Claim 16, lines 1-3). Considering that a tag storing unit is just something that stores an index or address, it is obvious that Tang teaches his limitation. Therefore, the Applicant's arguments are moot in view of the prior art.

12. Claim 6 is unpatentable for the reasons submitted for Claim 1.

13. With regards to Claim 8, the Applicant alleges that "Tang fails to disclose or suggest for the operation of searching the memory address from a tag-storing unit of the controller in response to the received read command". However, Tang states the following: "If the memory instruction is a memory read instruction or case=1, determine if the requested data is already stored inside the flash memory bridging device in step S430. If the requested data is in the flash memory bridging device, step S450 is executed to respond to the memory read instruction. On the other hand, if the requested data is not in the flash memory bridging device, step S440 is

executed to read the data from the NAND flash memory before executing step S450 to respond to the memory read instruction" (Section 0028, lines 11-20). Therefore, the Applicant's arguments are moot in view of the prior art.

14. With further regards to Claim 8, the Applicant alleges that "there nothing to suggest that the block address translation unit 345 is used for accessing the buffer region 310", and "there is nothing to suggest that the block address translation unit 345 would necessarily provide any sort of translation function to access the buffer region 310". However, Tang states "If the requested data is in the flash memory bridging device, step S450 is executed to respond to the memory read instruction" (Section 0028, lines 14-16). Step S450 is the response with readout data. Since this data is now bridged, the main control logic unit receives (is able to now read or write) it (as mentioned above). Therefore, the Applicant's arguments are moot in view of the prior art.

15. Claims 3-4 remain unchanged by the Applicant, and therefore stand rejected.

16. Claims 5 and 9-13 have been amended, but stand rejected in view of the prior art.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

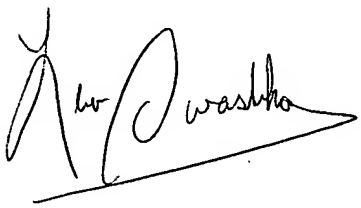
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on 9 Hours Schedule), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER